ABSTRACT OF THE DISCLOSURE

SRAMs A, B, C, and D having pixel data of each small block of each large block, for example a small block A_{ij} for the SRAM A, to simultaneously read out a plurality of pixel data in the small block by specifying an address assigned to each small block, and a matrix of coefficient in which a matrix of plural coefficients are arranged are provided. Also provided are a coefficient matrix controller 12 and an adding section 13 to multiply the plural coefficients respectively by pixel data corresponding to each thereof and obtain a sum of the multiplied results. Each pixel data of each small block forming one large block, the pixel data being read out from the SRAMs A, B, C, and D, are multiplied by the coefficient matrix rearranged into a predetermined order.